NARAYANA ENGINEERING COLLEGE::NELLORE

AUTONOMOUS

Department of Electronics & Communication Engineering

Date: 12/12/2022

REPORT on Career Opportunities in semiconductor Sector

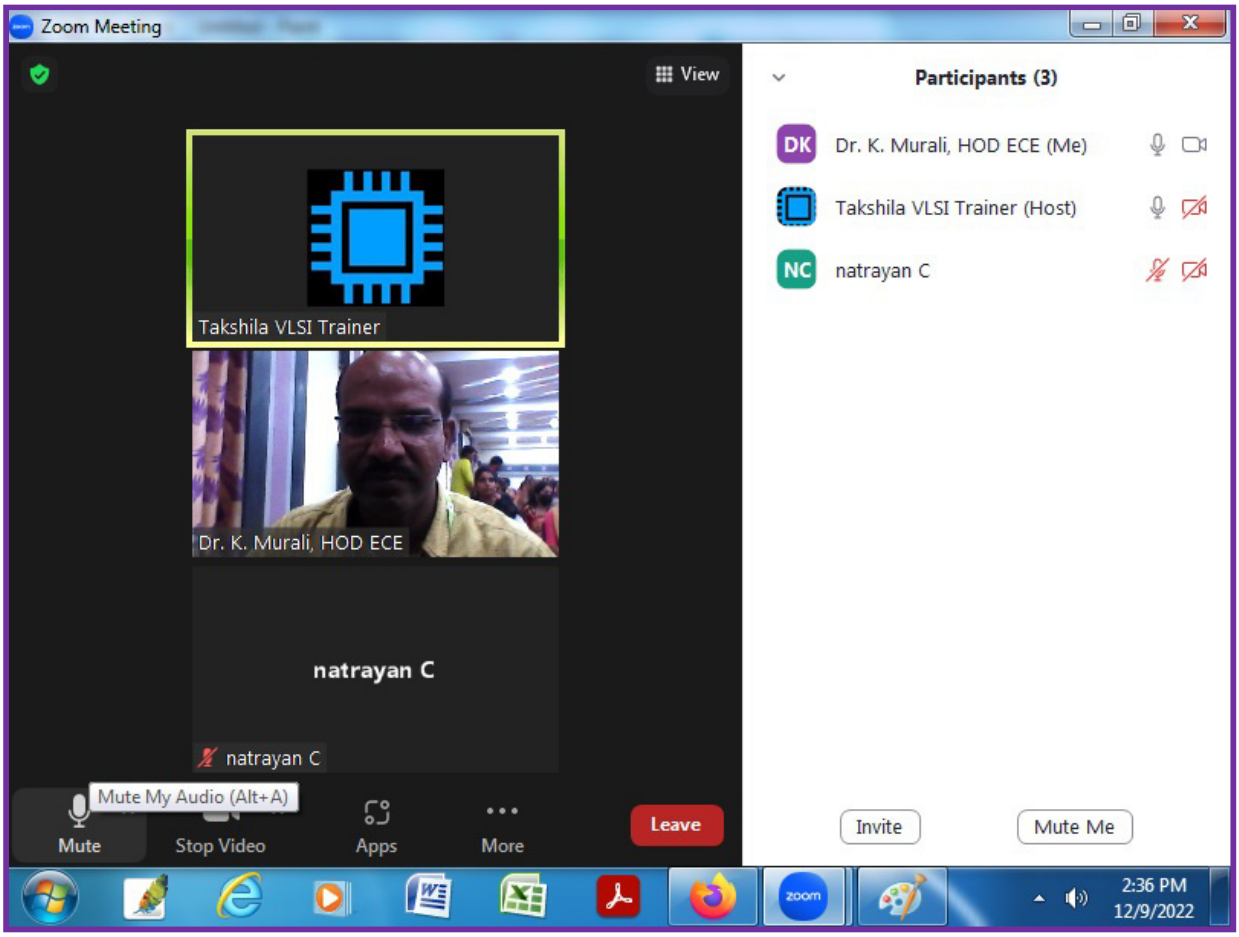
1	**Name of the Activity/Event**	Virtual Seminar on Career Opportunities in semiconductor Sector		
2	**Date of Activity/Event**	09/12/2022		
3	**Organized by/Name of the committee**	Dept. of Electronics & Communication Engineering		
4	**Place of Activity/event**	Narayana Engineering College, Nellore		
5	**Resource person/guest/organization**	Mr. Mahesh, Physical Design Engineer, Intel Technologies India Pvt. Ltd., Bangalore.		
6	**Type of activity/Event**	Virtual Seminar(IIIC)		
7	**Activity/Event objectives**	1. To provide an awareness about VLSI Core industries. 2. Outline the various Semiconductor Service Companies. 3. To summarize the various job opportunities in Semiconductor Sector.		
8	**Participation**	Students	Faculty	Total
		107	-	107
9	**General remarks**	The sessions are helpful to the students to select appropriate job in semiconductor sector.		
10	**Suggested Improvements**	-		
11	**Enclosures**	1. Request letter 2. Circulars 3. Report 4. Attendance		
12	**Signature of In charge/convener**			

A BRIEF DESCRIPTION OF THE EVENT:

Department of Electronics and Communication engineering had conducted a virtual seminar on "Career Opportunities in semiconductor Sector" under Industry Institute Interaction Cell (IIIC) for IV B.Tech students on 09-12-2022. The Resource Person for the event is Mr. Mahesh, Physical Design Engineer, Intel Technologies India Pvt. Ltd., Bangalore.

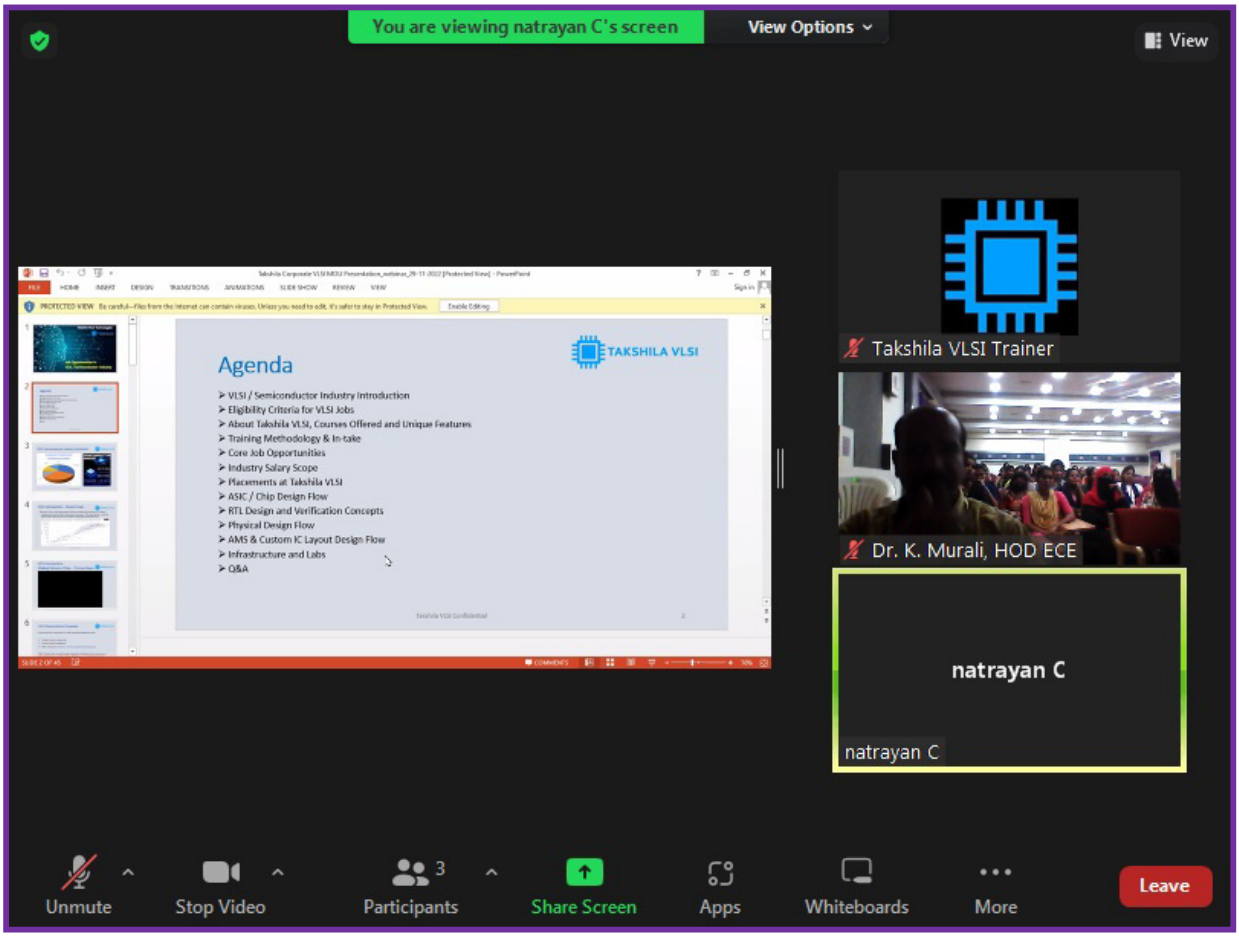
The session was inaugurated in the presence of Head of the Department, around 02:35 P.M on 09-12-2022. Dr. K. MURALI, Head of the ECE Department initiated the

session with motivating words and encouraged the students to be interactive during the session.

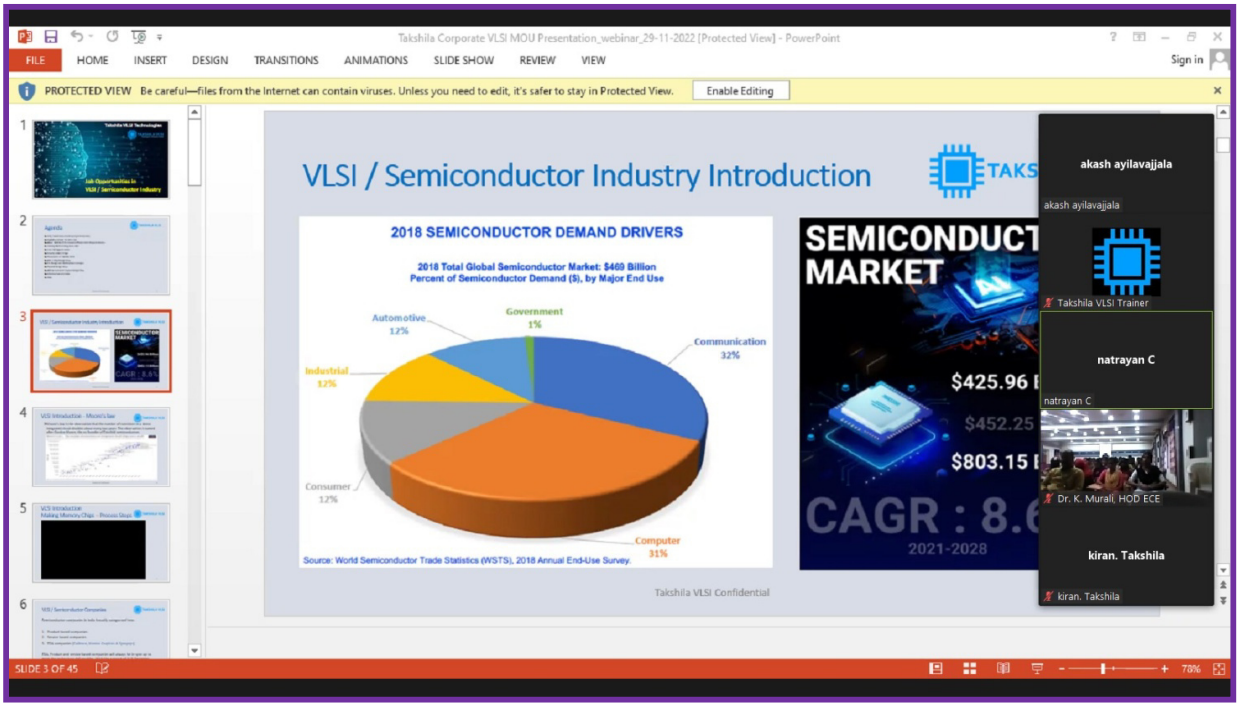


Dr. K. Murali introducing the Resource Person

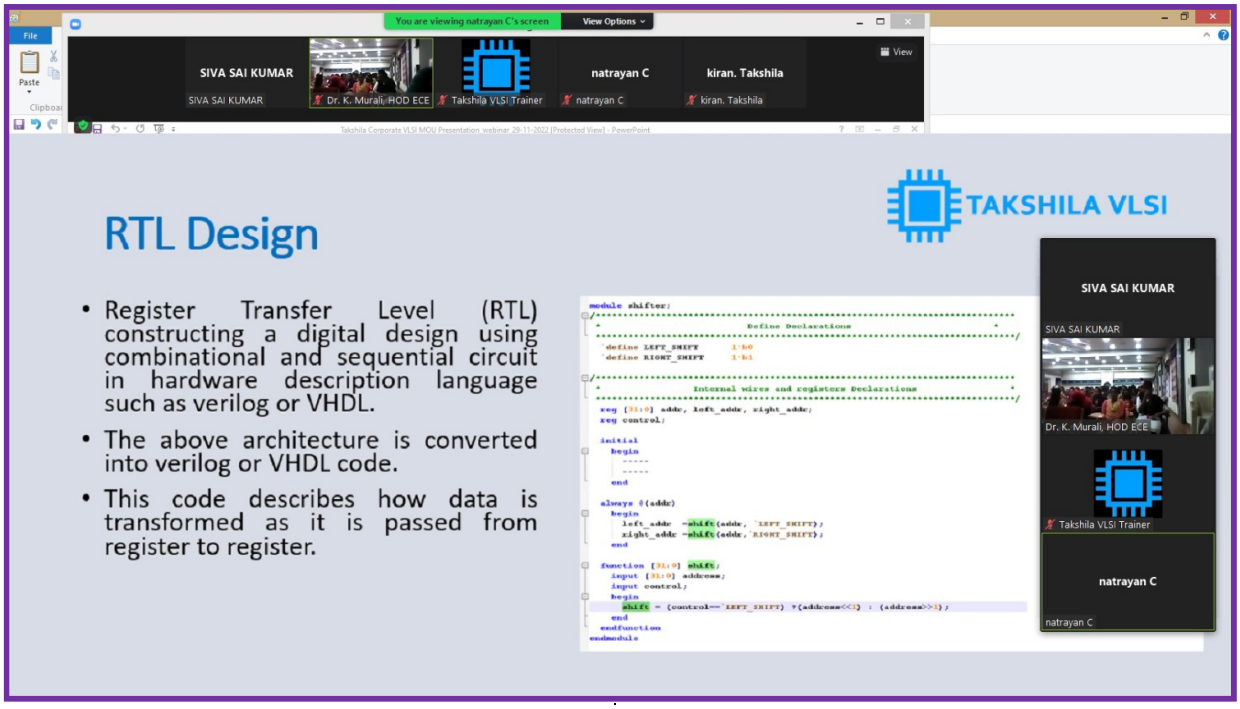
The semiconductor industry is the aggregate of companies engaged in the design and fabrication of semiconductors and semiconductor devices, such as transistors and integrated circuits. It formed around 1960, once the fabrication of semiconductor devices became a viable business. Very large-scale integration or VLSI is a process in which millions of MOS transistors are combined and integrated on a single semiconductor microchip. With the global semiconductor revenue crossing USD 440 Billion in 2020, there is an increasing need to design and produce highly efficient and specialized chips that can power new age technologies such as AI/ML, IoT, AR/VR, Cloud etc., which are increasingly becoming mainstream instead of remaining niche technologies. Growth in consumer electronics, computing devices, post pandemic, smartphones, intelligent vehicles etc., has further increased the demand.



Outlining the topics covered in Virtual Seminar

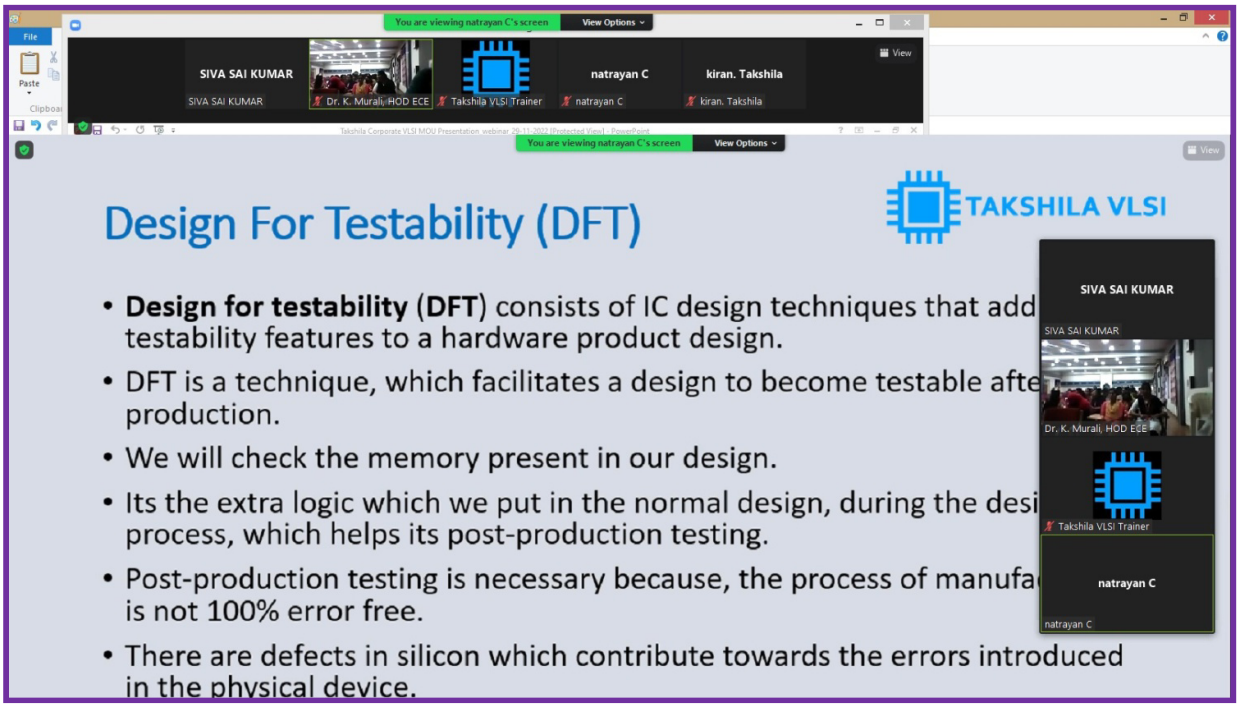


Explaining about the Semiconductor Market



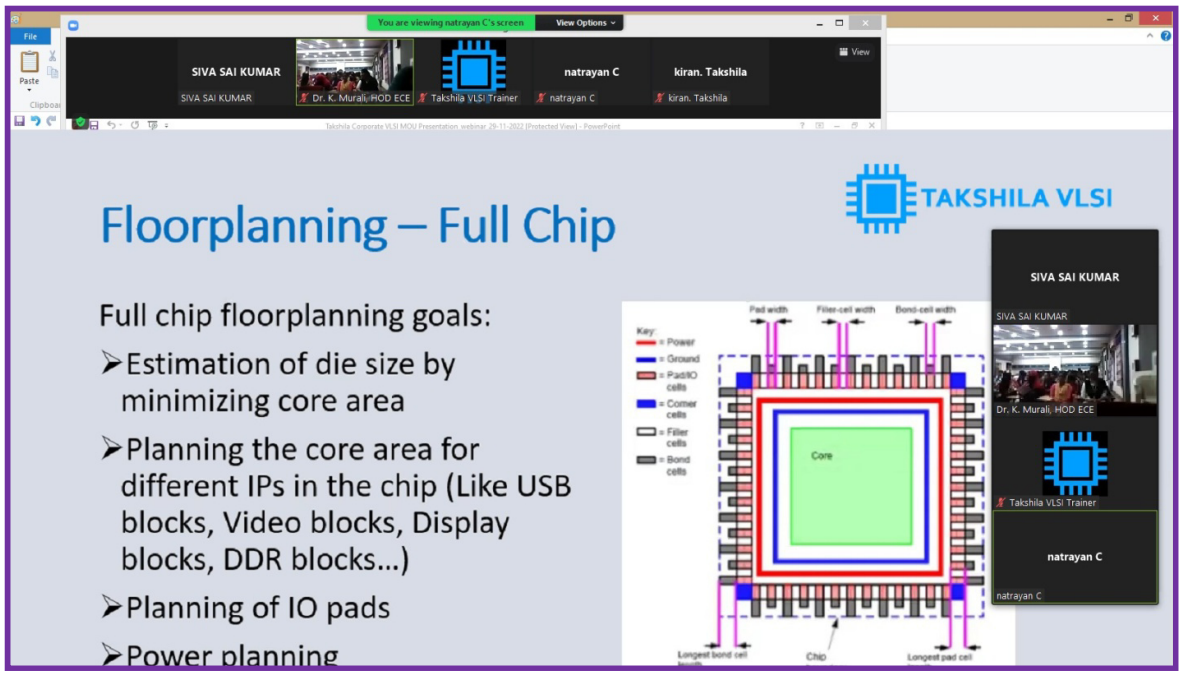
Explaining about the RTL Design

Design For Testability (or Design for Test, or DFT) refers to design techniques that make products easier to test. Examples include the addition of test points, parametric measurement devices, self-test diagnotics, test modes, and scan design.

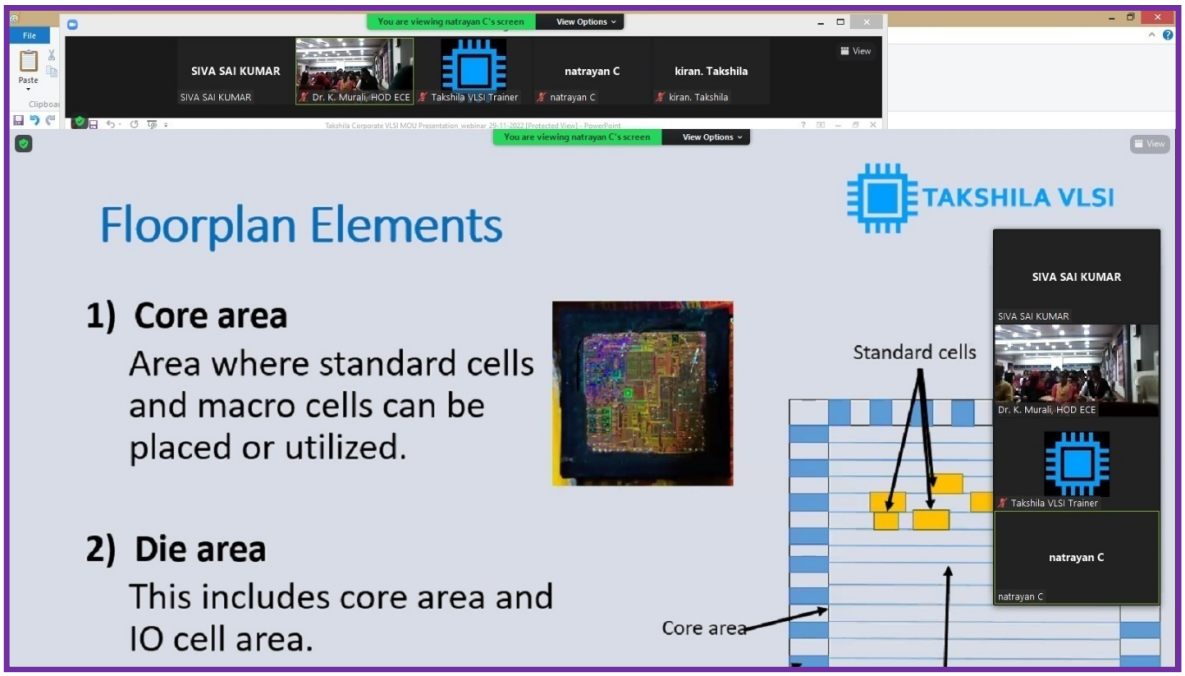


Explaining about Design for Testability

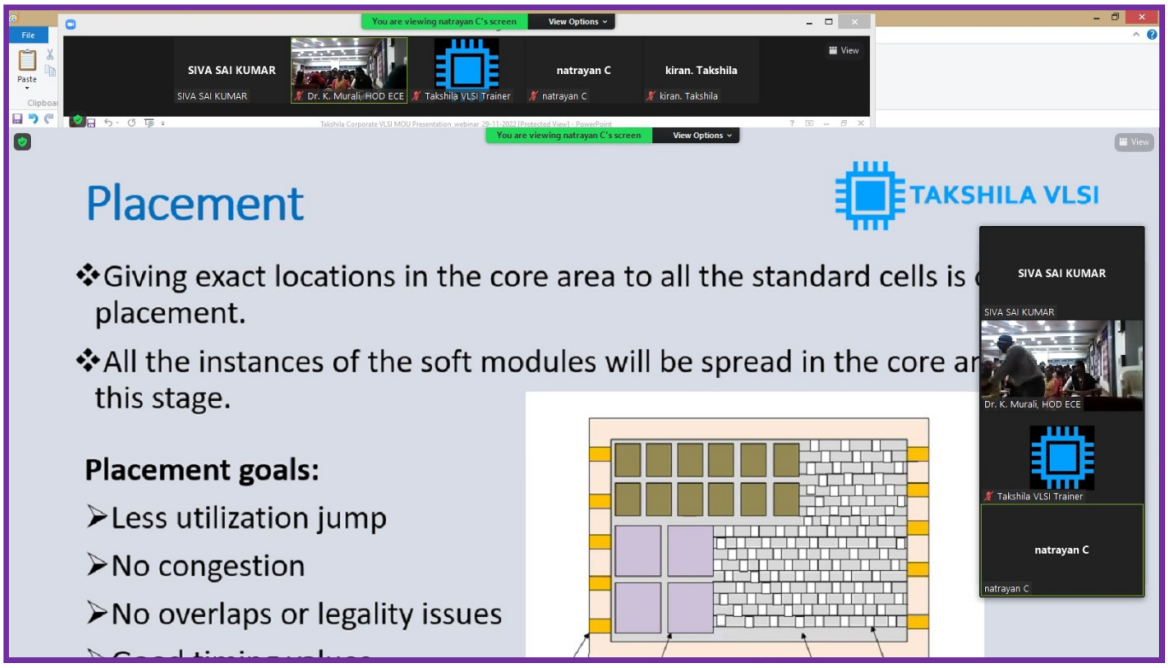
In the VLSI Physical Design Stage, Floorplanning is an essential step, as it is an effective means to manage circuit design complexity, which is increasing with the advancement in technology. Floorplanning involves determining the locations, shape, size of modules in a chip and as such it estimates the chip area, delay and the wiring congestion, thereby providing a ground work for layout. Placement is the process of placing the standard cells inside the core boundary in an optimal location. The tool tries to place the standard cell in such a way that the design should have minimal congestions and the best timing.



Explaining about Floor Planning

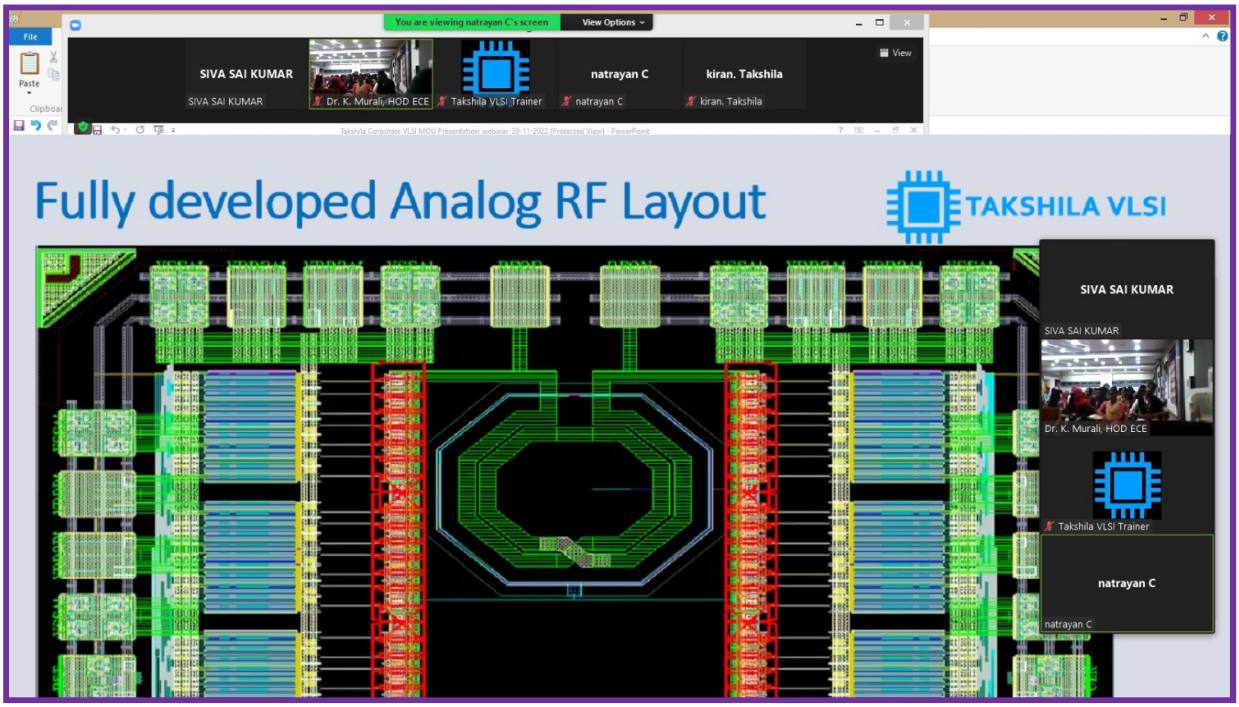


Explaining the elements of Floor plan



Explaining about Floor Planning

Explaining about Clock Tree Synthesis



Explaining about Analog RF Layout

Students Actively Participating in the Virtual Seminar

All the students participated actively and at the end some of the students asked queries about RTL Design, I/O Planning and the various opportunities in VLSI sector. The resource person clarified the queries of the students.

Total Number of Participants: 107

HOD ECE