



### Department of Electronics & Communication Engineering

Date: 12/12/2022

#### REPORT on Career Opportunities in semiconductor Sector

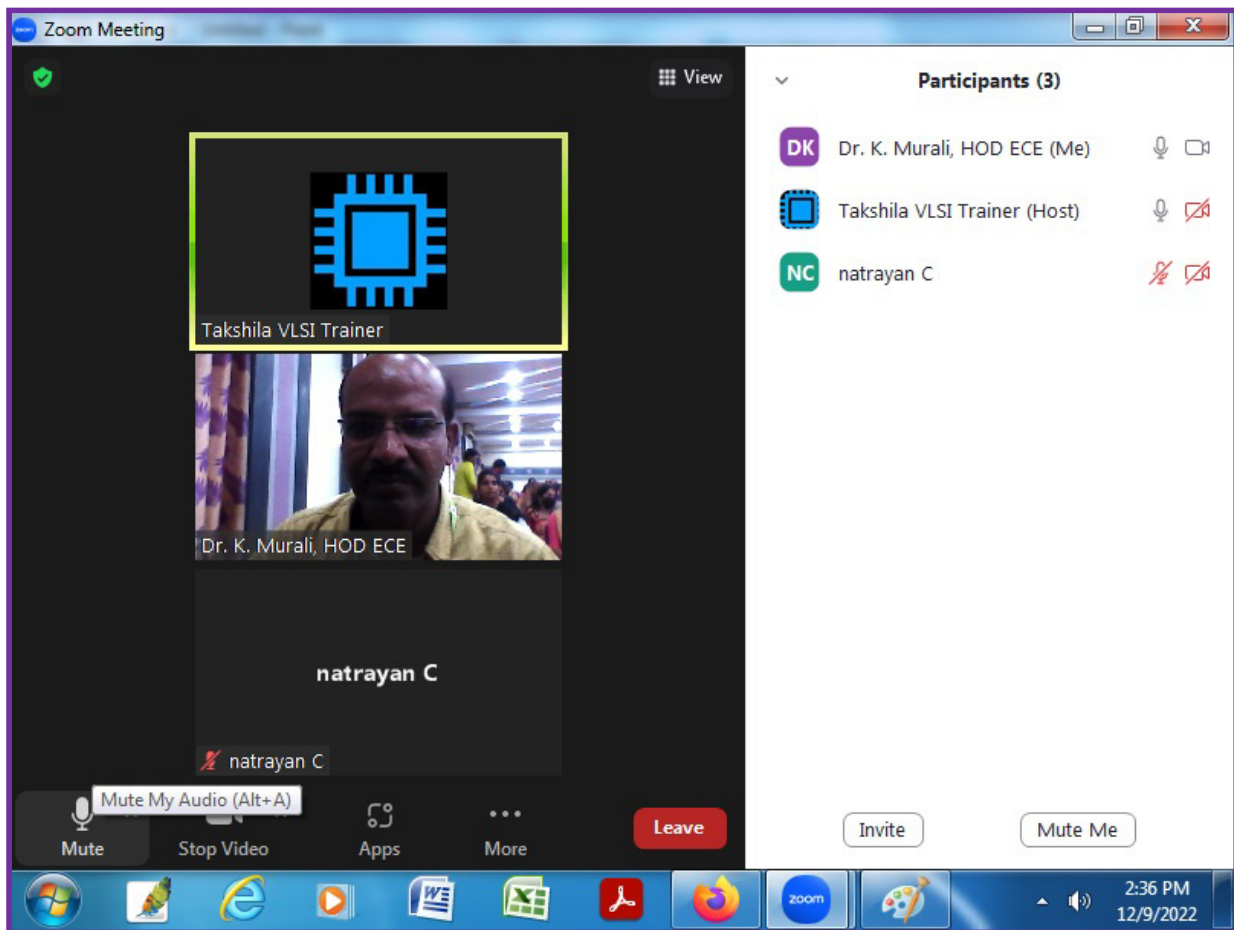
<b>1</b>	<b>Name of the Activity/Event</b>	Virtual Seminar on Career Opportunities in semiconductor Sector		
<b>2</b>	<b>Date of Activity/Event</b>	09/12/2022		
<b>3</b>	<b>Organized by/Name of the committee</b>	Dept. of Electronics & Communication Engineering		
<b>4</b>	<b>Place of Activity/event</b>	Narayana Engineering College, Nellore		
<b>5</b>	<b>Resource person/guest/organization</b>	Mr. Mahesh, Physical Design Engineer, Intel Technologies India Pvt. Ltd., Bangalore.		
<b>6</b>	<b>Type of activity/Event</b>	Virtual Seminar(IIIC)		
<b>7</b>	<b>Activity/Event objectives</b>	<ol style="list-style-type: none"> <li>1. To provide an awareness about VLSI Core industries.</li> <li>2. Outline the various Semiconductor Service Companies.</li> <li>3. To summarize the various job opportunities in Semiconductor Sector.</li> </ol>		
<b>8</b>	<b>Participation</b>	Students	Faculty	Total
		107	-	107
<b>9</b>	<b>General remarks</b>	The sessions are helpful to the students to select appropriate job in semiconductor sector.		
<b>10</b>	<b>Suggested Improvements</b>	-		
<b>11</b>	<b>Enclosures</b>	<ol style="list-style-type: none"> <li>1. Request letter</li> <li>2. Circulars</li> <li>3. Report</li> <li>4. Attendance</li> </ol>		
<b>12</b>	<b>Signature of In charge/convener</b>			

#### **A BRIEF DESCRIPTION OF THE EVENT:**

Department of Electronics and Communication engineering had conducted a virtual seminar on "Career Opportunities in semiconductor Sector" under Industry Institute Interaction Cell (IIIC) for IV B.Tech students on 09-12-2022. The Resource Person for the event is Mr. Mahesh, Physical Design Engineer, Intel Technologies India Pvt. Ltd., Bangalore.

The session was inaugurated in the presence of Head of the Department, around 02:35 P.M on 09-12-2022. Dr. K. MURALI, Head of the ECE Department initiated the

session with motivating words and encouraged the students to be interactive during the session.



### ***Dr. K. Murali introducing the Resource Person***

The semiconductor industry is the aggregate of companies engaged in the design and fabrication of semiconductors and semiconductor devices, such as transistors and integrated circuits. It formed around 1960, once the fabrication of semiconductor devices became a viable business. Very large-scale integration or VLSI is a process in which millions of MOS transistors are combined and integrated on a single semiconductor microchip. With the global semiconductor revenue crossing USD 440 Billion in 2020, there is an increasing need to design and produce highly efficient and specialized chips that can power new age technologies such as AI/ML, IoT, AR/VR, Cloud etc., which are increasingly becoming mainstream instead of remaining niche technologies. Growth in consumer electronics, computing devices, post pandemic, smartphones, intelligent vehicles etc., has further increased the demand.

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**Agenda**

- > VLSI / Semiconductor Industry Introduction
- > Eligibility Criteria for VLSI Jobs
- > About Takshila VLSI, Courses Offered and Unique Features
- > Training Methodology & In-take
- > Core Job Opportunities
- > Industry Salary Scope
- > Placements at Takshila VLSI
- > ASK / Chip Design Flow
- > RTL Design and Verification Concepts
- > Physical Design Flow
- > AMS & Custom IC Layout Design Flow
- > Infrastructure and Labs
- > Q&A

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Participants: 3

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***Outlining the topics covered in Virtual Seminar***

Takshila Corporate VLSI MOU Presentation\_webinar\_29-11-2022 [Protected View] - PowerPoint

FILE HOME INSERT DESIGN TRANSITIONS ANIMATIONS SLIDE SHOW REVIEW VIEW

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**VLSI / Semiconductor Industry Introduction**

**2018 SEMICONDUCTOR DEMAND DRIVERS**

2018 Total Global Semiconductor Market: \$469 Billion  
Percent of Semiconductor Demand (\$), by Major End Use

End Use	Percentage
Automotive	12%
Industrial	12%
Consumer	12%
Government	1%
Communication	32%
Computer	31%

Source: World Semiconductor Trade Statistics (WSTS), 2018 Annual End-Use Survey

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SEMICONDUCTOR MARKET

\$425.96  
\$452.25  
\$803.15

CAGR : 8.6%  
2021-2028

Participants: 4

akash ayilavajjala  
Takshila VLSI Trainer  
natrayan C  
Dr. K. Murali, HOD ECE  
kiran. Takshila

SLIDE 3 OF 45 78%

***Explaining about the Semiconductor Market***



In the VLSI Physical Design Stage, Floorplanning is an essential step, as it is an effective means to manage circuit design complexity, which is increasing with the advancement in technology. Floorplanning involves determining the locations, shape, size of modules in a chip and as such it estimates the chip area, delay and the wiring congestion, thereby providing a ground work for layout. Placement is the process of placing the standard cells inside the core boundary in an optimal location. The tool tries to place the standard cell in such a way that the design should have minimal congestions and the best timing.

**Floorplanning – Full Chip**

Full chip floorplanning goals:

- Estimation of die size by minimizing core area
- Planning the core area for different IPs in the chip (Like USB blocks, Video blocks, Display blocks, DDR blocks...)
- Planning of IO pads
- Power planning

The diagram shows a central green 'Core' area surrounded by a red 'Pad' layer, a blue 'Filler-cell' layer, and a black 'Bond-cell' layer. Labels include 'Longest bond cell width', 'Chip', and 'Longest pad cell'. A legend identifies: Pad (red), Ground (blue), Pad/IO cells (orange), Corner cells (yellow), Filler cells (grey), and Bond cells (black).

***Explaining about Floor Planning***

**Floorplan Elements**

- 1) Core area**  
Area where standard cells and macro cells can be placed or utilized.
- 2) Die area**  
This includes core area and IO cell area.

The diagram shows a grid representing the die area. A central region is labeled 'Core area' and contains several yellow blocks representing 'Standard cells'. The surrounding grid represents the IO cell area.

***Explaining the elements of Floor plan***

**Placement**

- ❖ Giving exact locations in the core area to all the standard cells is called as placement.
- ❖ All the instances of the soft modules will be spread in the core area during this stage.

**Placement goals:**

- Less utilization jump
- No congestion
- No overlaps or legality issues
- Good timing closure

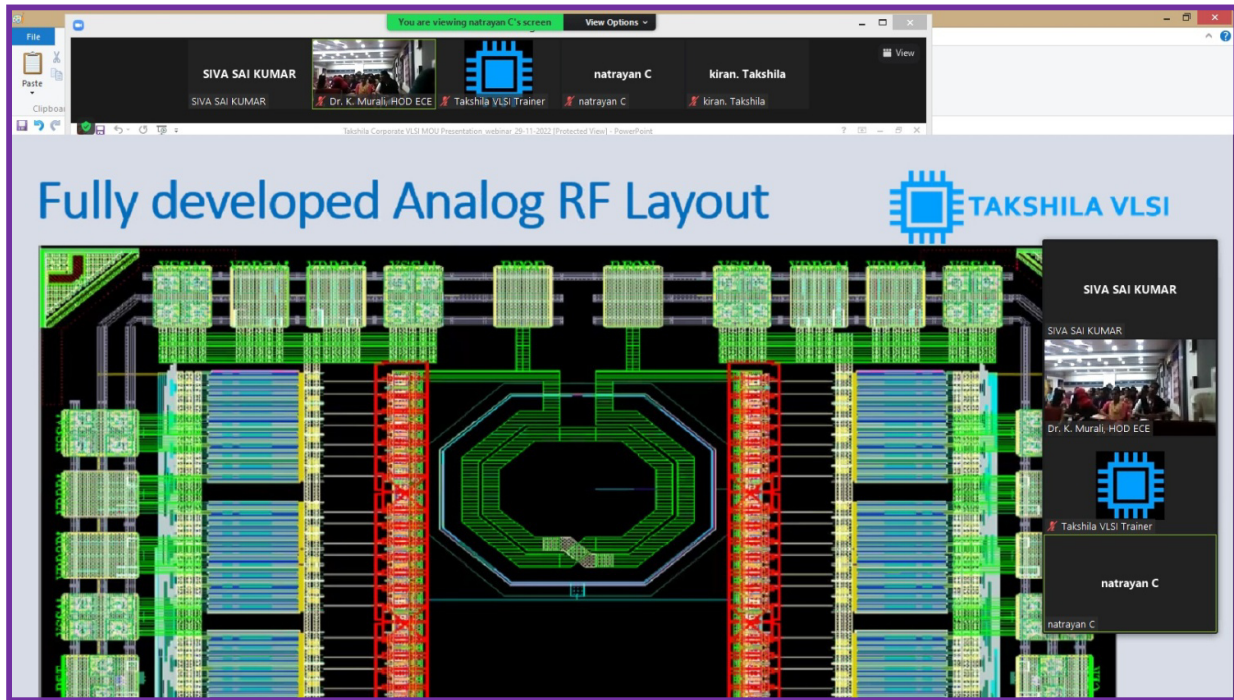
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SIVA SAI KUMAR  
Dr. K. Murali, HOD ECE  
Takshila VLSI Trainer  
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***Explaining about Floor Planning***



***Explaining about Clock Tree Synthesis***



***Explaining about Analog RF Layout***



***Students Actively Participating in the Virtual Seminar***

All the students participated actively and at the end some of the students asked queries about RTL Design, I/O Planning and the various opportunities in VLSI sector. The resource person clarified the queries of the students.

***Total Number of Participants: 107***

**HOD ECE**